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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,851	HANSEN, CRAIG	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 12-32 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

3. Claim 12 is directed to a computer readable medium having instructions that perform floating point operations on registers. Computer readable medium can be storage medium such as optical disk or a transmission medium such as a carrier wave. While instructions stored on computer readable storage medium may be meet the requirements to be statutory the disclosure does not limit the claimed invention to computer readable storage medium such as a memory. The other type of computer readable medium namely transmission medium does not provide instructions tangibly embodied so as to be executable. A transmission medium is not part any of the classes of invention (machine, manufacture, process, composition of matter). Therefore since the instruction on a transmission medium is not tangibly embodied the invention of claims 12 and the claims that depend on claim 12 (claims 13-22) are not statutory.

4. Claim 23, is directed to a computer data signal, a data signal that contains a instructions does not provide for instructions that are tangibly embodied so as to be executable. A data signal also is not one of the statutory classes of invention (machine, manufacture, composition of matter or process). Therefore the invention claims 23 and the claims that depend on claim 23 (claims 24-32) are not statutory.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1,2,4-13,15-24,26-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer (patent No. 6,823,353) in view of Kabir (patent No. 5,933,160).

7. Fischer taught the invention as claimed including a data processing ("DP") system comprising:

Decoding and executing instructions that instruct a computer system to perform operations (e.g., see col. 7, lines 16-35); at least some of the instructions including a group floating point instruction operating on first and second registers partitioned into a plurality of floating point operands, the floating point operands having a defined precision, having a defined result precision which is equal to the defined precision of the operands;(e.g., see fig. 6); at least some group floating-point instruction being a group floating-point multiply-and-add instruction(e.g., see fig. 10 and col. 2, lines 35-65) further operation on a third register partitioned into a plurality of floating point operands, operable to multiply the plurality of floating point operands in the first and second registers and add the plurality of floating-point operands in the third register, each producing a floating-point value to provide a plurality of floating-values ,each of the floating point values capable of being represented by the defined result precision, and a concatenated result having a plurality of partitioned fields for receiving the plurality of

floating point values (e.g., see col. 2, lines 35-65 and col. 8, lines 8-65 and col. 3, line 9-col. 10, line 44).

8. Fischer taught (claims 1,12,23) a plurality of different precisions for the operands but did not expressly detail the precision was dynamically variable (e.g,. see fig. 2a,3,6). Kabir however taught dynamically changeable precision the result (e.g., see fig. 5a,5b and col. 4, line 45-col. 6, line 5).

9. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Fischer and Kabir. Both references were directed to the problems of performing mathematics processing on data partitioned in registers (e.g,. see col. 2, lines 32-52 of Kabir and fig. 2a of Fischer). Fischer taught multiply add operation on portions operands that were less than the whole width of the register (e.g., see fig. 11). Consequently one of ordinary skill would have been motivated to incorporate the Kabir teaching of floating point arithmetic on portions of a register performed in parallel in a single clock cycle at least to increase the rate at which the floating point arithmetic operates and allows the system to be used in pixel processing applications and by providing efficient processing of pixel data (e.g., see col. 2, lines 28-52 of Kabir)

10. Claims 1 is representative of the other independent claims in the application. The method claim 1 provides the steps and features that are included in the corresponding claims 12 and 23. The difference in the claim 12 and 23 from claim 1, is that instructions are embodied in a computer readable medium (claim 12) and a signal (in claim 23). Clearly in order to implement the system Kabir and Fischer the instructions

and data would have had to have been stored in a readable medium such as a memory so that the instructions and data would not be lost. As to the limitation of the instruction being a signal clearly one of ordinary skill would have been motivated to provide the instructions via signal in order for upload or download the instructions to a computer for implementation of the Fischer, Cohen and Kabir system. Due to the similarities of the corresponding claims 1,12,23 these claims are rejected as detailed above.

11. As per claim 2,13,24 Fisher taught at least some of the group floating point instruction being at least one member of the collection consisting of group floating-point subtract, group floating-point add (e.g., see figs. 6,9), and group floating point multiply(e.g, see fig. 2b), operable to perform a subtract (e.g., see figs. 2b,11), add and multiply respectively on the plurality of floating point operands in the first and second registers, each producing a floating point value to provide a plurality of floating point values(e.g., see fig. 3 and col. 10, lines 9, line 8-col. 10, line 55), each of the floating point values capable of being represented by the defined result precision, and a concatenated result having a plurality of partitioned fields for receiving the plurality of floating point values (e.g., see fig. 2a,3,6,9); and at least some group floating point instruction being one memory of the collection consisting of group floating point set less and group floating point set greater than or equal operable to perform a set less than or set greater than operation respectively on the plurality of floating point operands in the first and second registers (e.g., see col. 12, lines 31-57)[the system shifts the operands by a predetermined number of bits e.g., 16 bits to place the operation in a portion of the register greater than or less than a position in the register then can contain other

operands], each producing a value to provide a plurality of values each of the values capable of being represented by the defined result precision, and a concatenated result having a plurality of partitioned fields for receiving the plurality of values (e.g,. see fig. 7),; and at least some of the instructions comprising data manipulations on multiple operands stored in partitioned fields wherein the data manipulations comprise copying and rearranging operands (e.g., see col. 9, lines 13-44 and col. 10, line 56-col. 11, line 11).

12. Fischer and Kabir did not expressly detail wherein the value zero if the operation produces a false result, and wherein the value identity if the value produces and true result. However this limitation is merely a view of the data and does not change the operation or structure of the system. Since in floating point arithmetic it was well known in the art that error such a (denormal data or overflow) would produce invalid data and prior art systems have provided validity indications for floating point results one of ordinary skill would have been motivated to at least provide an indication as to validity of the floating results (although the claims does not require this indication) where a high value would indicate validity and low value would invalidity of floating point results. On the other hand since Fischer and Kabir taught partitioning of the data in the registers it would had been obvious to use of a mask to generate the partitioned data for transfer of only a portion of the data in a register from one register to another register wherein a mask was well known to provide ones and zeros for the bits in a register that were either transferred of masked out.

13. As per claim 4,15,26 Fischer and Kabir did not expressly detail a width of 128 bit. However since the industry standard processors have increased word widths by a multiples of 2 at least as the memory sizes have increase to be able to address the larger amounts of memory. Therefore one of ordinary skill would have been motivated to use a 128 bit word width to be able to address the larger size memories that would store the data operated on by the Fischer system.

14. As per claim 5,16 Fisher taught the concatenated results were provided to a register (e.g., see fig. 2a and col. 8, lines 8-32) Kabir also taught this limitation (e.g., see figs. 5a,5b and col. 8, lines 21-56).

15. As per claim 6,8,17,19,27,29 Kabir taught use of a defined precision of 16 bits and 32 bits (e.g., see figs 5a,5b). Fisher and Kabir did not specifically detail 64-bit precision. However when larger register widths would have been used in systems that used larger registers and amounts of memory to take advantage of the industry wide reduction in cost of memory one of ordinary skill would have been motivated use 64 bit with at least in the operations that used half the register in when a 128 bit register was used (this corresponds the operations that used half the register ,16 bits of a 32 bit register in Kabir (e.g., see fig. 5b of Kabir).

16. As per claim 7,18,28, Fisher taught sign bits, significand and exponent bits (e.g., see col. 1, lines 30-40 and col. 15 ,lines 47-57). As to the specifically claims arrangement of data in claim 7,9,11 does not alter the operation of the claimed invention as no specific change in the apparatus or steps performed is claimed. Since the data in the registers of Fisher and Kabir comprise bits and the claimed data

comprises bits therefore the only different is the view of the data. Since these differences are found in non-functional descriptive material and are not functionally involved in the steps recited. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see in re Gulack, 703, F 2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983) ; In re Lowry, 32, F 3d 1579, 32 USPQ2d 1031 (Fed Cir. 1994). Therefore it would have been obvious to a person of ordinary skill in the art at the time of the invention to perform the floating point operations on partial width data in defined width in any format of floating point data because such data does not functionally relate to the steps in the method claimed and because the subjective interpretation of the data does not patentably distinguish the claimed invention.

17. Claims 3,14,25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer and Kabir as applied to claims 1,2,4-13,15-24,26-32 above, and further in view of Cohen (patent No. 5,751,614).

18. As per claim 3, Cohen taught the zero value and the identify value are values that construct a mask operable to select between alternative expressions using bit-wise Boolean operation (e.g., see fig. 3).

19. It would have been obvious to one of ordinary skill to combine the teachings of Fischer and Cohen. Both Fischer and Cohen were directed to performing operations of data in portions of data from a register (e.g., see fig. 3 of Cohen and fig. 2a of Fisher). Cohen taught a system for generating separating the portions of data in a register for transfer and partial width operations. Therefore one of ordinary skill would have been

motivated to incorporate partial width data generation teaching of Cohen using a mask in the Fischer system that operated on partial width data at least to efficiently processing of the data of different width including shifting the data (e.g., see col. 10, lines 47-67 and col. 2, lines 60-col. 3, line 34 of Cohen).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Van Hook (patent No. 5,933,157) disclosed a central processing unit with integrated graphics functions operating on partitioned data (e.g., see abstract and fig. 2,4,5,7c, 8b, 8c, 8d, 8e, 8f, 8g, 9b, 11b).

Yung (patent No. 5,996,066) disclosed a partitioned multiply and add/subtract instruction for CPU (e.g., see abstract).

Sidwell (patent No. 6,145,077) disclosed a system for manipulation of data (e.g., see fig. 6,6).

Miura (patent No. 5,327,543) disclosed a system for selectively masking operand portions for processing (e.g., see abstract and 2,3,4,,5,8,9).

Abdallah (patent No. 6,115,812) disclosed a system for vertical SIMD computations (e.g., see figs. 1, 2,3a, 3b, 3c, 5a, 5b, 6a, 6b, 7a, 7b).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

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PRIMARY EXAMINER